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A resonant soliton scheme to implement ultrafast optical logic gates using semiconductor nonlinear directional couplers (NLDC) has been investigated numerically. It has been demonstrated that the resonant soliton logic gates meet fundamental requirements for digital optical logic devices: logic level restoration, cascadability, and logical completeness.

The operation of AND, OR, XOR, NOT, NOR, and NAND logic gates have been demonstrated in numerical simulations using 2 X 2 device configuration for a directional coupler. 3 X 3 NLDC design has been suggested to implement logically complete gates without necessity to cascade two or more couplers. Using 3 X 3 device configuration, an inventor (NOT gate) and a NOR gate have been implemented.

The opening characteristics of the resonant soliton logic gates have been investigated numerically using 100 fs input pulses with 2 (pie) pulse area. It has been shown that the operating speed of all constructed gates is 2 Tbit/s, the operation is bit-rate flexible, the signal-to-noise ratio is generally higher than 4, and the latency is on picosecond timescale. Quantitative comparison between the operating characteristics of the resonant soliton logic gates and the corresponding parameters of NOLM gates (fiber optics) and also semiconductor electronic logic gates has been made. A conclusion has been drawn that the resonant soliton logic gates represent a novel and unique class of all-optical devices which are capable to operate at least 100 times faster than the most advanced electronic gates.

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Ultrafast optical logic with semiconductor nonlinear directional couplers

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Content

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1. Outline of the accomplished tasks

A major goal of the performed research work has been to demonstrate numerically that the resonant soliton switches satisfy the fundamental requirements for digital optical logic devices and permit various logic gate functions in the same way how the electronic switches do. In the performed numerical simulations, the issues of logic level restoration, cascadability, and logical completeness with the resonant soliton scheme have been addressed. It has been shown that the resonant soliton switches meet these three requirements for digital optical logic devices.

The operation of AND, OR, XOR, NOT, NOR and NAND logic gates have been modelled using 2×2 arm branching design for a nonlinear directional coupler (NLDC). 3×3 NLDC design has been suggested to implement logically complete gates without necessity to cascade two or more 2×2 couplers. Using 3×3 device configuration, the operation of an inverter (NOT gate) and a NOR gate have been demonstrated. The operating characteristics of the resonant soliton logic gates have been assessed and compared with those of a nonlinear optical loop mirrow configuration (fiber optics) and also with semiconductor electronic logic gates.

2. Numerical method

A basic numerical code describing the operation of a semiconductor NLDC in the resonant excitation regime has been developed in our recent work [1] where the inherent features of ultrafast all-optical resonant switching have been investigated. This code applies to a directional coupler with two-arm branches (2×2 NLDC). The mathematical formalism is briefly described below.

Based on a coupled-mode approach, we solve the reduced Maxwell-semiconductor Bloch equations (MSBE) for single-mode waveguides in the case of resonant excitation at the $1s$-exciton resonance:

$$\frac{\partial E_j(\xi,\eta)}{\partial \xi} = i\frac{2\pi}{c^2}\frac{\omega_L^2}{k_L}P_j(\xi,\eta) + iKE_l(\xi,\eta), \tag{1}$$

$$\frac{\partial P_j(\xi,\eta)}{\partial \eta} = -i\left[\beta_1|P_j(\xi,\eta)|^2 - i\gamma_2\right]P_j(\xi,\eta) + \frac{id_{cv}}{2\hbar}\left[1-\beta_2|P_j(\xi,\eta)|^2\right]E_j(\xi,\eta), \tag{2}$$

where $E(\xi,\eta)$ and $P(\xi,\eta)$ are complex amplitudes of the electric field and the induced polarization in the

moving coordinate frame ($\xi = z$ is the propagation coordinate, $\eta = t - z/U$ is the time coordinate, U is the group velocity of the pulse), β_1 and β_2 are nonlinear exchange and phase-space filling parameters, γ_2 is a phenomenological dephasing rate, $j, l = 1, 2$ ($j \neq l$), and K is a coupling coefficient. The model assumes a large exciton binding energy, thus allowing higher exciton and continuum states to be neglected. For femtosecond light pulses with moderate intensities, the neglect of screening is justified.

In the numerical simulations, the material parameters of II-VI CdZnTe/ZnTe MQWs have been used [2]. It should be emphasized that qualitative results do not depend on the choice of the semiconductor material parameters. If III–V GaAs/AlGaAs MQWs material parameters are used, the carrier wavelength will be different, but only a minor quantitative change in the operating characteristics of the resonant couplers (such as switching speed, switching contrast ratio, etc.) occurs.

Eqs. (1)–(2) have been solved using the fourth-order Runge-Kutta method which had been described in our previous work [1,3]. The input has been given by various sequences of sech-shaped pulses $E(\xi = 0, \eta) = E_0 sech(\eta/\tau)$. The duration of each pulse has been chosen to be $\tau = 100$ fs (intensity FWHM), and the time delay between the consecutive pulses – 500 fs. The interaction of the signal pulses in channel 1 and the control pulses in channel 2 of NLDC has been monitored by computing the pulse intensity profile, the pulse energy, and the pulse area transmitted through each channel. In the case of cascading of two NLDCs, the same MSBE approach (1)–(2) has been used, where the output of the first coupler has served as an input for the second one.

So far, we have treated a directional coupler with two-arm branches (2×2). In order to analyze the operation of a more complex three-arm branch (3×3) with three input ports and three output ports, an extended numerical code has been developed and tested. The 3×3 device configuration is less conventional than the 2×2 one [4]. The schematic of 3×3 NLDC as well as the motivation for its use in comparison with 2×2 branching coupler is discussed in Section 4. Coupled-mode equations describing the 3×3 system are an extension of Eqs. (1)–(2), namely

$$\frac{\partial E_1(\xi,\eta)}{\partial \xi} = i\frac{2\pi}{c^2}\frac{\omega_L^2}{k_L}P_1(\xi,\eta) + iKE_2(\xi,\eta) + iK'E_3(\xi,\eta), \tag{3}$$

$$\frac{\partial E_2(\xi,\eta)}{\partial \xi} = i\frac{2\pi}{c^2}\frac{\omega_L^2}{k_L}P_2(\xi,\eta) + iKE_1(\xi,\eta) + iKE_3(\xi,\eta), \tag{4}$$

$$\frac{\partial E_3(\xi,\eta)}{\partial \xi} = i\frac{2\pi}{c^2}\frac{\omega_L^2}{k_L}P_3(\xi,\eta) + iKE_2(\xi,\eta) + iK'E_1(\xi,\eta), \tag{5}$$

$$\frac{\partial P_j(\xi,\eta)}{\partial \eta} = -i\left[\beta_1|P_j(\xi,\eta)|^2 - i\gamma_2\right]P_j(\xi,\eta) + \frac{id_{cv}}{2\hbar}\left[1-\beta_2|P_j(\xi,\eta)|^2\right]E_j(\xi,\eta), \tag{6}$$

where $j = 1, 2, 3$; K' is a coupling coefficient between two outer waveguides (1 and 3), and the rest of the parameters are the same as in Eqs. (1)–(2).

Eqs. (3)–(6) have been solved using the same procedure as in the case of Eqs. (1)–(2) (the fourth-order Runge-Kutta method). All numerical simulations have been performed using the existing computer facilities of the Department of Theoretical Physics, Australian National University: Unix DEC Alpha Workstations with the operating speed up to 500 MHz. The numerical codes have been written in FORTRAN77.

3. Requirements for digital optical logic gates

The fundamental properties required by a digital electronic or optical logic device are gain (logic level restoration), cascadability, and logical completeness. These three issues have been addressed in the performed numerical simulations, and the results are presented below.

Logic level restoration

A gain is required to compensate the signal degradation due to loss or crosstalk, and restore signals to the values which represent valid logic states. In the case of digital signal processing which is of interest here, the binary logic states "1" and "0" can be identified using a threshold detection: a pulse with amplitude above the threshold represents "1" whereas a pulse with amplitude below the threshold (or no signal at all) represents "0". For example, the input in Figure 1 is given by a packet "1110111".

In a semiconductor NLDC, the major cause of the pulse attenuation is the presence of strong dephasing processes. The latter ones are characterized in our model by the polarization dephasing time T_2 (or dephasing rate $g_2 = 1/T_2$) which is compared with the input pulse duration τ ($\tau = 100$ fs in the performed numerical simulations): $T_2 \gg \tau$ corresponds to weak dephasing regime, $T_2 \sim \tau$ corresponds to strong dephasing regime.

The general principle which allows to amplify the signals all-optically in the semiconductor NLDC is demonstrated in Figure 1. The main idea is to use the interaction between the resonant solitons which have

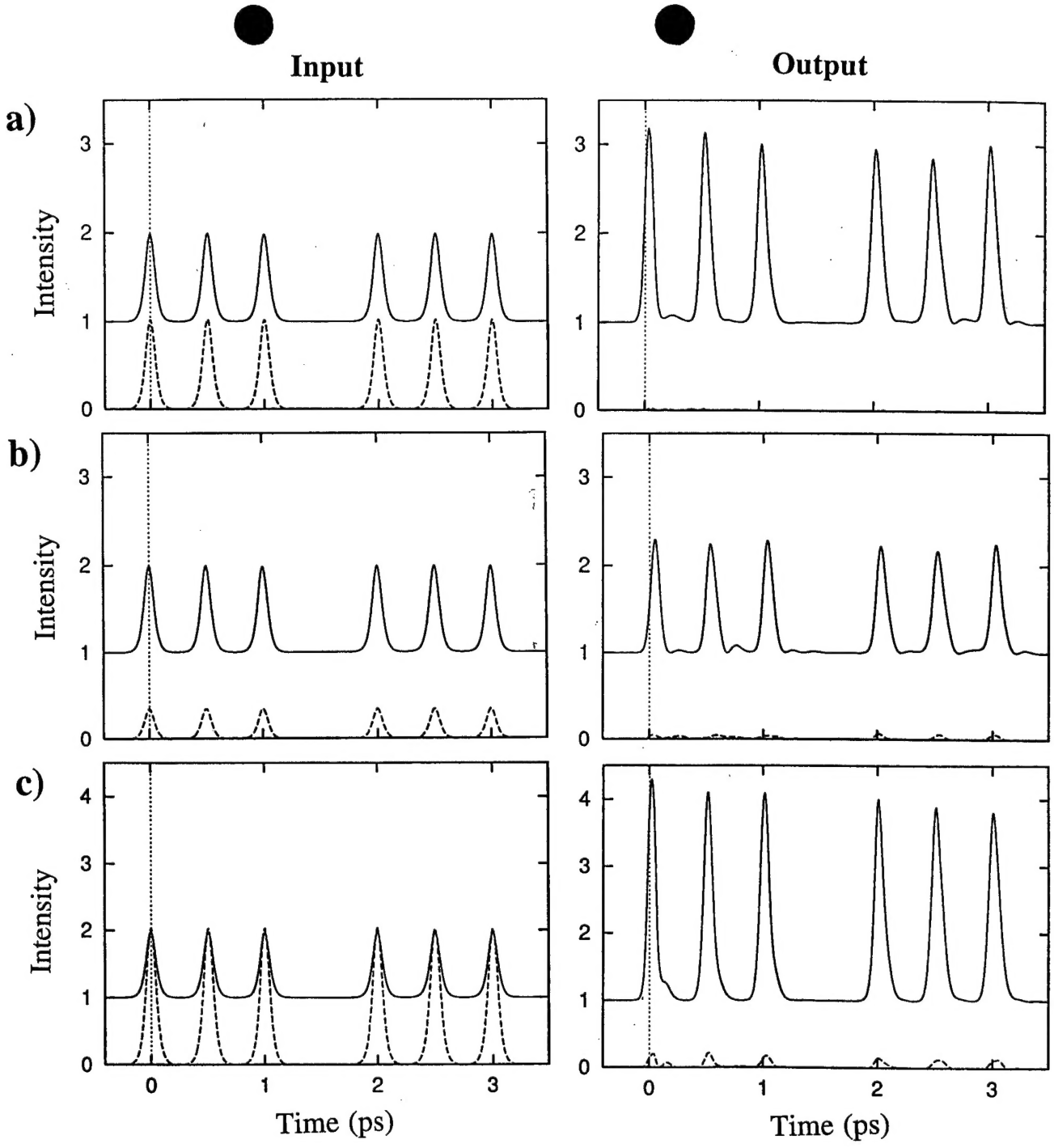


FIG. 1. (a) All-optical signal amplification using the interaction of signal pulses in channel 1 (solid line which is shifted up for clarity) and control pulses in channel 2 (dashed line). The signal and control pulses have a phase mismatch of $\Delta\phi = +\pi/2$. No dephasing processes are taken into account ($g_2 = 0$). The coupler length is $d = L_c/2$. The input of NLDC is shown on the left side of the Figure, the output - on the right side. All intensity values are normalized to the input pulse intensity. (a) The signal and control pulses have equal amplitudes. The gain factor (signal out/signal in) is two. (b) The strong signal and weak control pulses interact: the gain is less than two. (c) The control pulses have twice the amplitude of the signal pulses: the gain factor is three.

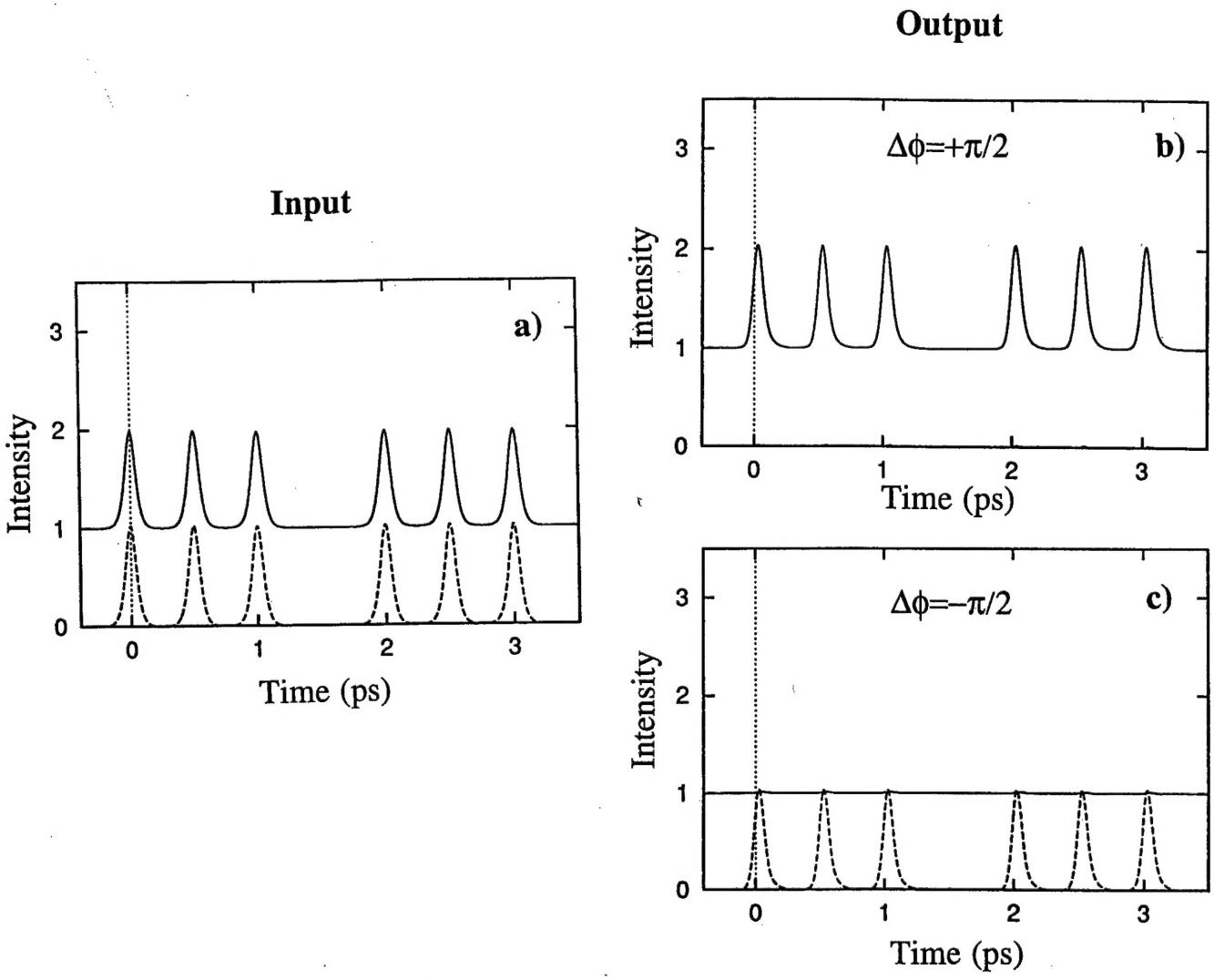


FIG. 2. Demonstration of logic level restoration and routing switching in the resonant NLDC. The dephasing time is $T_2 = 200\ fs$. The interaction between the signal and control pulses restores the signal logic level to its original (input) value which is shown in (a). (b) If the phase mismatch between the interacting pulses is $\Delta\phi = +\pi/2$, the output goes to the channel 1. (c) If $\Delta\phi = -\pi/2$, the output goes to the channel 2.

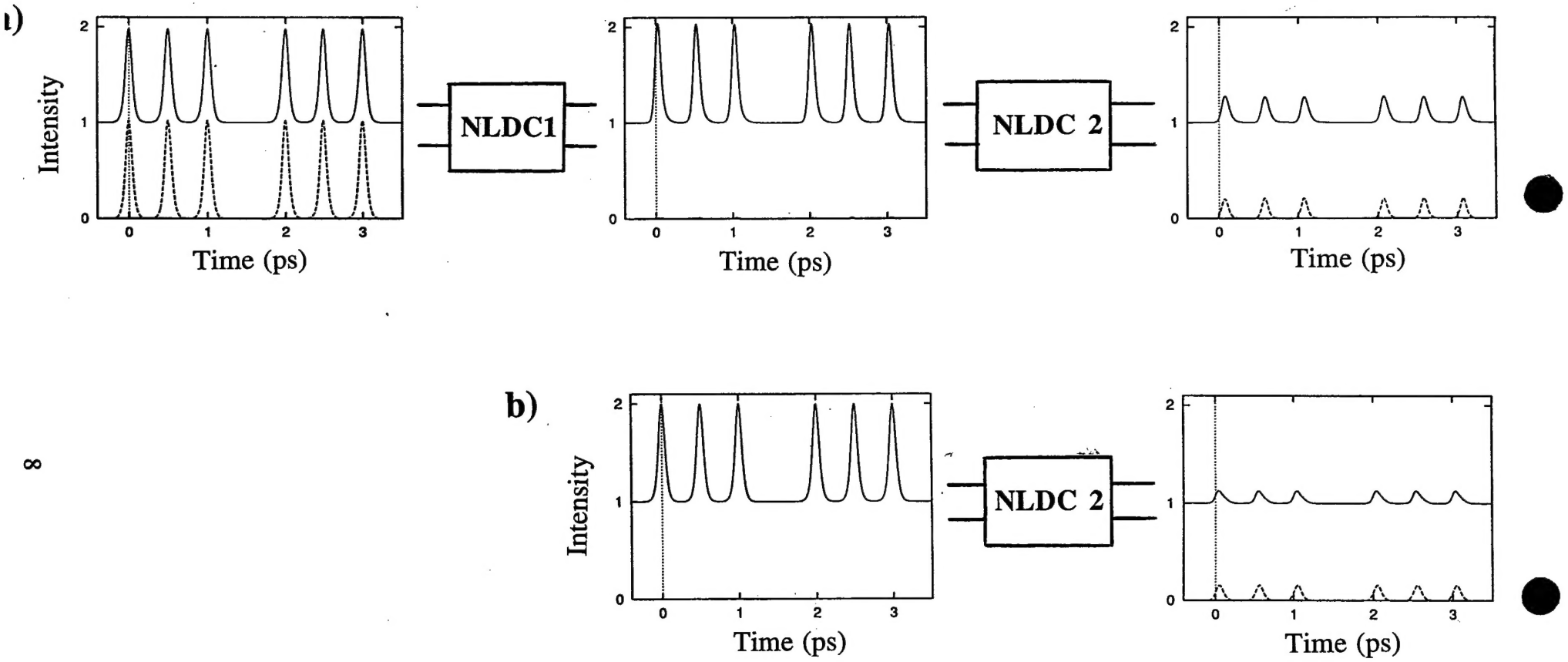


FIG. 3. (a) A cascade of two resonant soliton switches. The output of NLDC1 serves as an input for NLDC2 provided that the signal logic level has been restored in NLDC1 ($T_2 = 200\ fs$). (b) For comparison, the outcome of a single NLDC2 for the input of the same format is shown.

a phase mismatch of $\pi/2$. Note that this approach is only applicable if the length of NLDC is chosen to be $d = L_c/2$ where L_c is the full-coupling length. Figure 1a shows that, in the case of interacting equal-amplitude solitons with the phase mismatch $\Delta\phi = \phi_2 - \phi_1 = +\pi/2$, the gain factor (signal out/signal in) is two. A smaller gain can be achieved when a strong and weak pulses interact (Figure 1b), and the gain factor larger than two results from the interaction of the signal pulses with the higher-amplitude control pulses (Figure 1c). The ideal case with no dephasing processes has been shown in Figure 1 to demonstrate the full potential of the amplification technique. When the dephasing is present, depending on its strength, the amplitude of the control pulses can be adjusted to achieve the output of NLDC of the same format as the input. For example, in the case of very strong dephasing $T_2 = 200$ fs which causes 50% signal attenuation in NLDC with no gain, the interaction between the equal-amplitude signal and control pulse restores the signal logic level to its original value (see Figure 2). In addition to the gain, the choice of sign in the phase mismatch $\Delta\phi$ of the interacting solitons allows to direct the signal in either of two output ports: if $\Delta\phi = +\pi/2$, the output goes to the channel $1'$ (Figure 2b); if $\Delta\phi = -\pi/2$, the output goes to the channel $2'$ (Figure 2c). In this implementation, the resonant NLDC simultaneously provides gain and operates as a routing switch.

It is important to note that the original phase of the signal pulses can be arbitrary. The amplification technique described above only requires a certain phase mismatch (namely, $\pi/2$) between the signal and control pulses. Due to robustness of the scheme (see [1]), the deviations up to $\sim 20\%$ from the required $\Delta\phi = \pi/2$ for the control pulses still allow efficient device operation.

Cascadability

Cascadability means that the output of one NLDC can directly drive the input to the next one, thus allowing the direct implementation of multi-level logic. The inputs and outputs of the same format are therefore key to allowing cascadability.

In the performed numerical simulations, a possibility to cascade the resonant soliton switches has been demonstrated. Figure 3a shows that an output of one coupler (NLDC1) can serve as an input for the next coupler (NLDC2) provided that the signal logic level has been restored in NLDC1. For comparison, an outcome of a single NLDC2 for the input of the same format is shown as well (Figure 3b). The output

of NLDC2 in both cases is essentially the same. This comparison proves that there is no change in the pulse carrier frequency after passing through the resonant soliton coupler. This is important because any substantial soliton self-frequency shift would lead to a severe signal degradation due to cascading. Note that the logic level restoration has been performed only in NLDC1 to have inputs of the same amplitude for NLDC2 in the cases with and without cascading (Figures 3a and 3b, respectively), therefore allowing direct comparison of NLDC2 operation in both cases. The signal attenuation after passing through NLDC2 is due to the presence of strong dephasing processes ($T_2 = 200$ fs) which, in contrast to NLDC1, have not been compensated for in NLDC2 by supplying the gain. Also note that the implementation shown in Figure 3b can be used as a broadcast or buffer switch which provides multiple copies of the input.

Although the resonant soliton scheme allows cascadability, the extend of cascading should be kept as low as possible. There are two main reasons to do so: (i) to minimize the ordinary propagation losses; (ii) to increase compactness of the setup making it more viable for applications. In Section 4, we demonstrate that a cascading of two or more 2×2 NLDCs is not the only possible way to implement complex logic functions, such as, for example, NOT and NOR. We show that the same functions can be achieved without a necessity to cascade the couplers if a 3×3 NLDC is used instead of conventional 2×2 directional couplers.

Logical completeness

A complete set of logic functions must include inversion which is a basic function of MOSFET electronics [5]. Here, we demonstrate a possibility of the inversion operation in the resonant soliton coupler using a phase-control method. The advantage of this simple approach which is illustrated in Figure 4 is that no clock stream is required to invert a signal. When the input is given by a signal "0" bit and a control "0" bit (half-amplitude pulses below the threshold) with the phase mismatch between the signal and control pulses $\Delta\phi = +\pi/2$, then the output of the coupler is "1" as a full-amplitude signal (above threshold) is transmitted through the channel $1'$ (we assume that only the output in channel $1'$ is used for signal processing; the output in channel $2'$ is discarded). When the input is given by a signal "1" bit and a control "1" bit with $\Delta\phi = -\pi/2$, then the output of the coupler is "0" as no signal is transmitted through the channel $1'$. Only the ideal case with no dephasing ($g_2 = 0$) is shown in Figure 4.

The scheme presented in Figure 4 is not the only possible way to implement the inversion function in

the resonant soliton switch. Another approach which is discussed in detail in the next Section is to use a clock stream. A necessity to supply the clock pulses would increase technical complexity of actual setups, but, on the other hand, it would increase their functionality as the clock pulses can also be used for logic level restoration (see an example of a NOT gate with gain in Section 4).

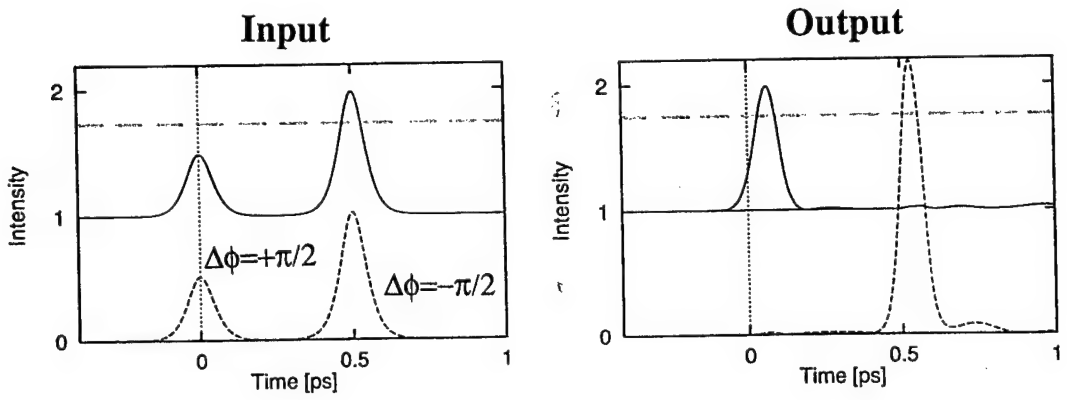


FIG. 4. Possibility of the inversion function in the resonant NLDC using the phase-control method. The channel $1'$ is chosen as an output port of NLDC. When the input is given by a signal "0" bit and a control "0" bit (half-amplitude pulses below the threshold which is shown by green dashed line) with $\Delta\phi = +\pi/2$, the output is "1" as a full-amplitude signal (above the threshold) is transmitted through the channel $1'$. When the input is given by a signal "1" bit and a control "1" bit with $\Delta\phi = -\pi/2$, the output is "0" as no signal is transmitted through channel $1'$.

4. The resonant soliton logic gates and their operating characteristics

We now proceed to the major goal of the project – construction of a variety of optical logic gates using the resonant soliton scheme. Below, we demonstrate that simple logic functions, such as AND, OR, and XOR, can be implemented in a single 2×2 NLDC. Complex logic functions, such as NOT, NOR, and NAND, require a cascade of two or more 2×2 NLDCs to be implemented or, alternatively, a single 3×3 NLDC can be used.

AND, OR, and XOR gates

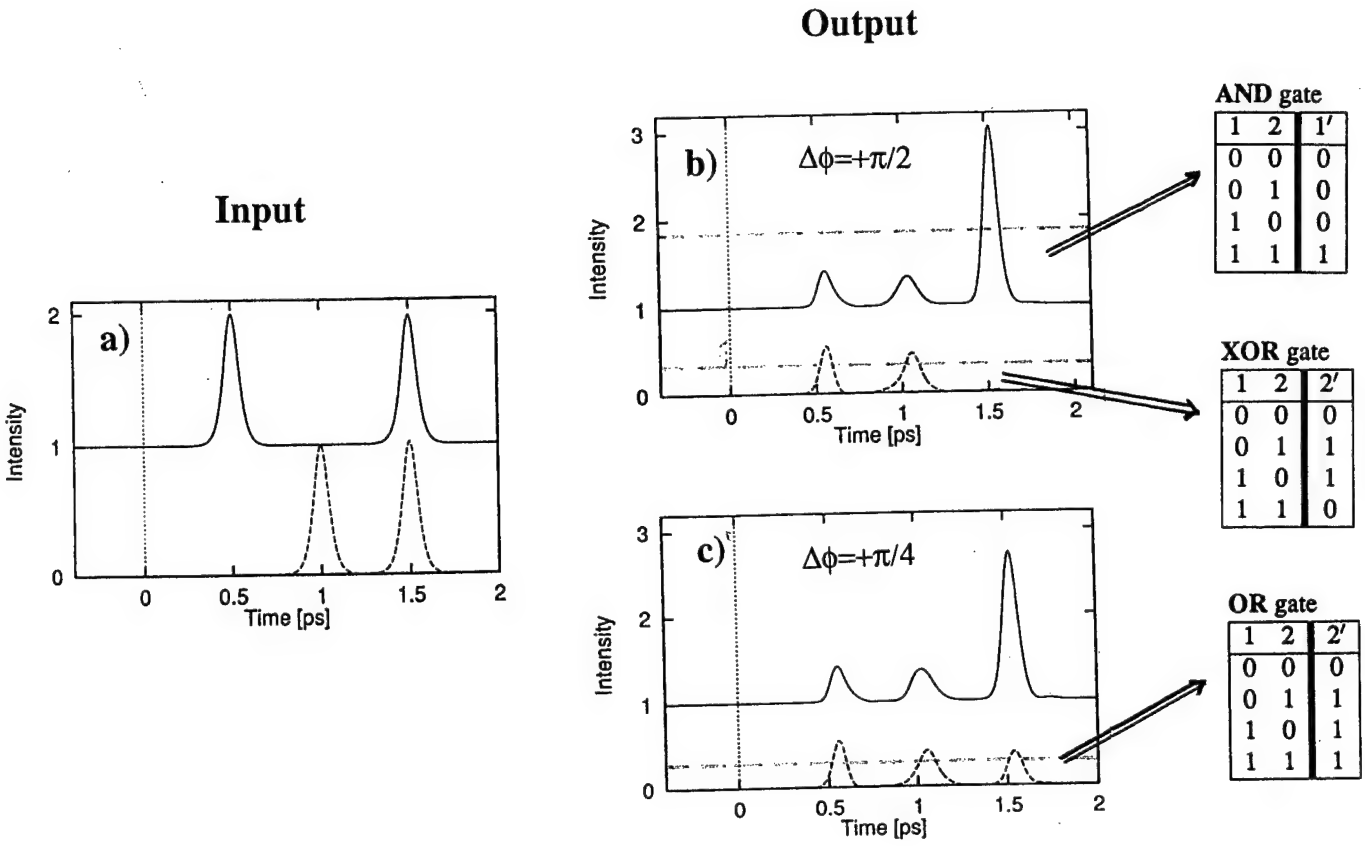
AND, OR and XOR gates do not perform an inversion operation, nevertheless they are frequently used within multi-logic networks. To demonstrate the basic principle how to achieve these different logic functions in a single NLDC, we first consider the ideal case with no dephasing ($g_2 = 0$).

In Figure 5, we show how AND, OR, and XOR logic functions can be implemented in a 2×2 NLDC. Figure 5a shows the input of the NLDC which is a logic stream "0101" in the channel 1 and a logic stream "0011" in the channel 2 (this gives all possible combinations of inputs for the gate, namely, 0:0, 1:0, 0:1, and 1:1). In Figure 5b, the output in channel $1'$ corresponds to AND gate operation: the output is "1" only when both inputs are "1", otherwise the output is "0". The output in channel $2'$ corresponds to XOR gate operation provided that the threshold detection level is adjusted to a lower value: the output is "0" only when both inputs are "0" or both inputs are "1", otherwise the output is "1". If we choose the phase mismatch between the signal and control pulses to be $\pi/4$ instead of $\pi/2$ (see Figure 5c), then the output in channel $2'$ corresponds to OR gate operation: the output is "0" only when both inputs are "0", otherwise the output is "1".

As seen from Figure 5b, AND gate simultaneously provides gain for the transmitted "1" bits. To amplify the outcoming "1" bits in XOR and OR gates (see Figures 5b and 5c) to the standard (input) value, an additional hardware is required. This could be a second cascaded NLDC where clock pulses are supplied. The amplification procedure is straightforward using the approach described in Section 3.

Inverter (NOT gate)

The ability to construct a NOT gate is crucial to verify the Boolean complete functionality of the resonant soliton switches. The inversion operation should also be achieved in a practically sensible way to make



1	2	1′
0	0	0
0	1	0
1	0	0
1	1	1

1	2	2′
0	0	0
0	1	1
1	0	1
1	1	0

1	2	2′
0	0	0
0	1	1
1	0	1
1	1	1

FIG. 5. Operation of AND, OR, and XOR gates and the corresponding truth tables. (a) The input of NLDC is a logic stream "0101" in the channel 1 and a logic stream "0011" in the channel 2. (b) $\Delta\phi = \pi/2$. The output in channel 1′ corresponds to AND gate operation: the output is "1" only when both inputs are "1", otherwise the output is "0". The output in channel 2′ corresponds to XOR gate operation provided that the threshold detection level (green dashed line) is adjusted to a lower value: the output is "0" only when both inputs are "0" or both inputs are "1", otherwise the output is "1". (c) $\Delta\phi = \pi/4$. The output in channel 2′ corresponds to OR gate operation: the output is "0" only when both inputs are "0", otherwise the output is "1".

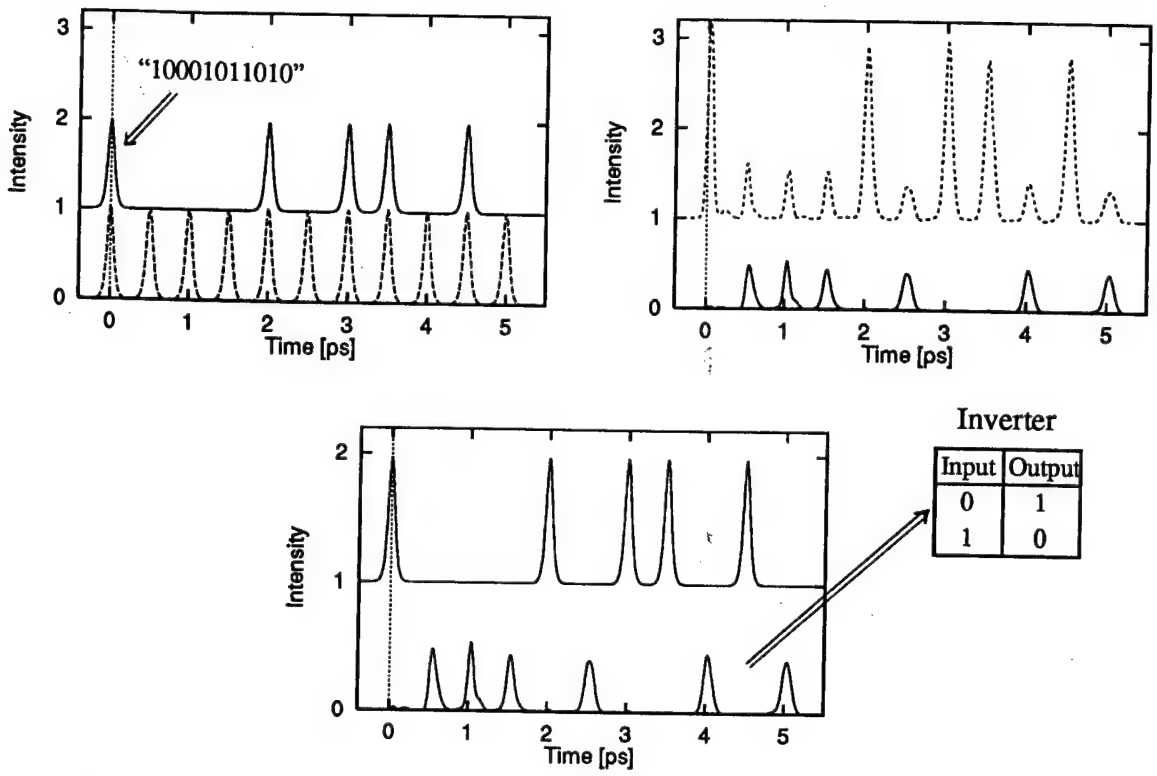
switches viable for potential applications in the packet networks. While a possibility to invert the signal has been demonstrated in Section 3, we believe that the approach shown there (see Figure 4) may not be the best suited for actual device implementations. This is because the sign of the phase mismatch, $\Delta\phi$, for the control pulses in channel 2 is supposed to be changed from $+\pi/2$ to $-\pi/2$ depending on the input value of the signal pulses. This change is easy to do numerically, but experimentally it would require additional hardware. Therefore, here we propose a different approach to construct a NOT gate.

In Figure 6, the operation of a NOT gate is demonstrated using a conventional 2×2 device configuration for directional couplers. The inversion operation occurs as a result of the interaction of the signal pulses (the input logic stream "10001011010" in channel 1) with the clock pulses (channel 2) which are $+\pi/2$ out of phase with the signal pulses. The multi-bit input packet is used to assess the operating speed of the gate and also to make the results relevant to signal processing in optical packet networks. The inverted logic stream "01110100101" is transmitted through channel $2'$ which is chosen as an output port of the gate (the output in channel $1'$ is discarded). In the case $g_2 = 0$, an operation of the NOT gate without gain (see Figure 6) gives NOT output which is not of the same format as the input because the outcoming "1" bits have lower amplitude in comparison with the input "1" bits. The use of higher amplitude clock pulses allows to restore the logic level to its standart (input) value (see Figure 6, NOT with gain) even in the presence of dephasing processes with $T_2 = 400$ fs. Note that a variation in the amplitude of the clock pulses can be used as a routine procedure for logic level restoration not only in NOT gate, but also in NOR and NAND gates as discussed below.

NOR and NAND gates

If the same device configuration as above (2×2 NLDC) is exploited, a cascade of three couplers is required to implement NOR and NAND functions. A schematic of this cascade and its operation at every stage are shown in Figure 7. The input of every NLDC is shown on the left side of Figure 7: the logic stream 1 is given by an 11-bit packet "10001011010" (NLDC1, solid line); the logic stream 2 is given by an 11-bit packet "11101011001" (NLDC2, solid line); clock pulses are shown by dashed line; the inverted logic streams enter NLDC3. The output of every NLDC is shown on the right side of Figure 7: the inverted logic stream 1 "01110100101" (NLDC1, solid line); the inverted logic stream 2 "00010100110" (NLDC2, solid

NOT without gain:



NOT with gain:

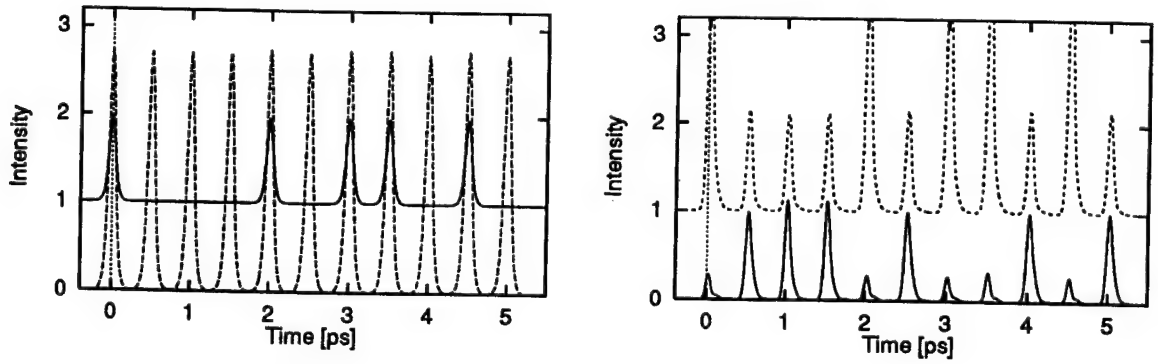
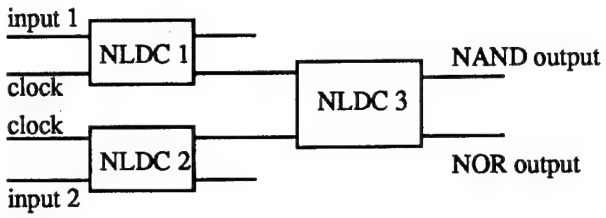
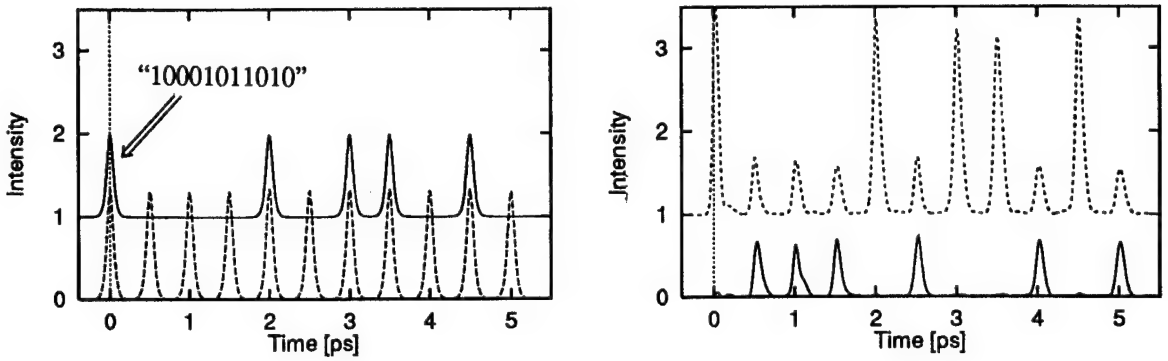


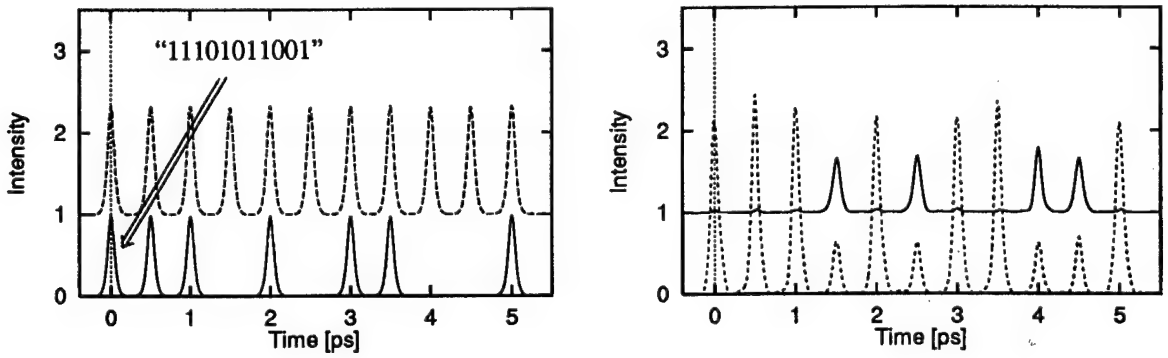
FIG. 6. NOT gate operation and the corresponding truth table. Top: NOT without gain. The input logic stream is given by an 11-bit packet "10001011010" (solid line, channel 1); the clock stream is shown by a dashed line. The clock pulses are $+\pi/2$ out of phase with the signal pulses. NOT output is shown by solid line (channel 2′); the output in the other channel is discarded (dotted line). $T_2 = \infty$; the signal and clock pulses have the same amplitude I_0; NOT output has the amplitude $0.5I_0$. Middle: The same as above, except only input and NOT output are shown with the corresponding truth table. Bottom: NOT with gain. $T_2 = 400$ fs; the amplitude of the clock pulses is $2.7I_0$; NOT output has the same amplitude I_0 as the input logic stream.



NLDC 1:



NLDC 2:



NLDC 3:

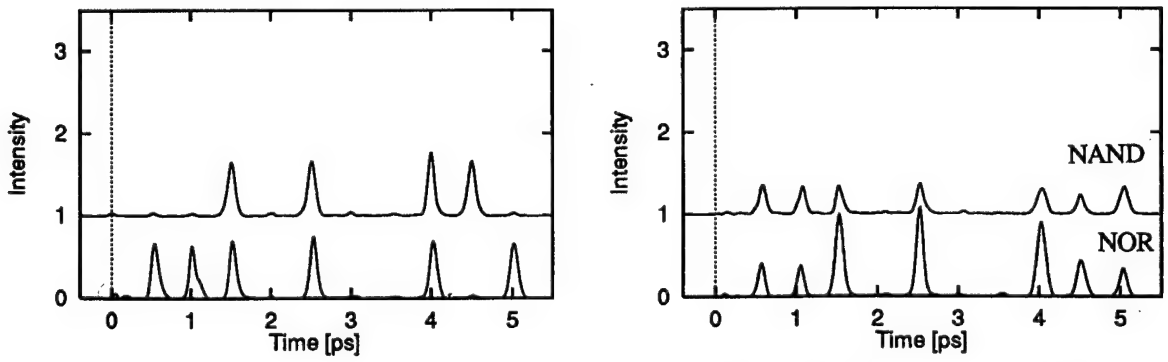


FIG. 7. Top: Schematic of a cascade of three NLDCs. Below: NOR and NAND gate operation. The input of every NLDC is shown on the left side: the logic stream 1 is given by an 11-bit packet "10001011010" (NLDC1, solid line); the logic stream 2 is given by an 11-bit packet "11101011001" (NLDC2, solid line); clock pulses are shown by dashed line; the inverted logic streams enter NLDC3. The output of every NLDC is shown on the right side: the inverted logic stream 1 (NLDC1, solid line); the inverted logic stream 2 (NLDC2, solid line); the discarded signal is shown by dotted line; NAND output in channel 1′ and NOR output in channel 2′ are shown by solid line (NLDC3).

line); discarded signals are shown by dotted line; NAND output "01110100111" in channel 1′ and NOR output "00010100100" in channel 2′ are shown by solid line (NLDC3). In the case of NAND gate, if both inputs are "0", the output is "1"; if both inputs have different logic values (one is "1" and another one is "0"), the output is "1"; if both inputs are "1", the output is "0". In the case of NOR gate, if both inputs are "0", the output is "1"; if both inputs have different logic values (one is "1" and another one is "0"), the output is "0"; if both inputs are "1", the output is "0". Figure 8 summarizes the results shown in Figure 7 – only input logic streams and NAND and NOR outputs with the corresponding truth tables are shown.

Note that no dephasing processes ($g_2 = 0$) are taken into account in Figures 7 and 8. The logic level restoration for NAND and NOR gates can be performed in the same way as for the NOT gate discussed above (*i.e.* adjusting the amplitude of the clock pulses).

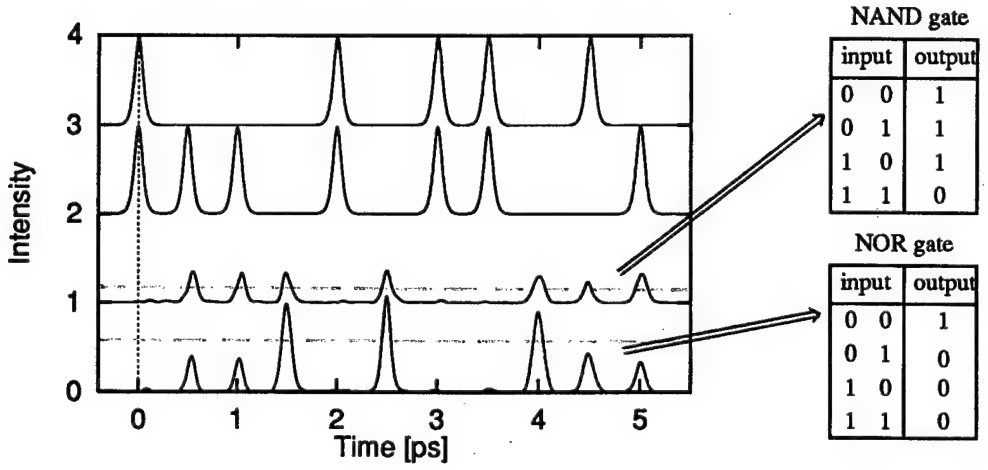


FIG. 8. NOR and NAND gate operation and the corresponding truth tables. The results of Figure 7 are summarized: only two inputs and NAND and NOR outputs are shown (the results are shifted vertically for clarity). The horizontal green line shows a threshold for amplitude detection.

NOT and NOR gates using 3×3 NLDC

Here, we demonstrate an operation of NOT and NOR logic gates using a different device configuration, namely, 3×3 NLDC. The main motivation to use this configuration instead of the conventional 2×2 NLDC is that it eliminates the necessity to cascade two or more couplers to implement the inversion operation and complex Boolean functions such as, for example, NOR. This may be a significant advantage for applications in optical computing where compactness of the gates is vital. Although 3×3 NLDC is a more complex device than 2×2 NLDC, it can be fabricated using the same lithography technique as for 2×2 semiconductor NLDC [6], with minor modifications.

A schematic of the 3×3 arm branching directional coupler is shown in Figure 9. The input packet 1 enters NLDC through one of the three input ports (for example, channel 1), the input packet 2 – through another one (for example, channel 3). The inputs are given by three-bit packets instead of a single pulse to assess the operating speed of the device. Channel 2 supplies the clock stream which is always present, even if both input packets are empty ("000", see Figure 9a). The input pulses in channels 1 and 3 are chosen to be in phase ($\Delta\phi_{13} = 0$) whereas the clock pulses are out of phase with the input pulses, $\Delta\phi_{12} = \Delta\phi_{32} = -\pi/2$. Under these chosen input conditions, the energy exchange between the three channels of NLDC as a function of the propagation distance has been computed solving Eqs. (3)–(6) from Section 2. The results are shown in Figures 9a-c. There is a periodic energy exchange between the channels with a characteristic period which depends on the coupling coefficients K, K', and the area of the input pulses. While the oscillations in energy are simple to understand in the cases of symmetric inputs (see Figures 9a and 9c), the results are more complex in the cases of nonsymmetric inputs (see Figure 9b).

Although no analytical treatment of the 3×3 NLDC operation has been attempted during the course of this project, the numerical investigation is sufficient to demonstrate that 3×3 NLDC permits various logic gate function. If we choose channel $2'$ as an output port of the NLDC and discard the outputs in the other two channels ($1'$ and $3'$), then, as seen from the numerical results in Figures 9a and 9c, a NOT output is achieved in certain range of propagation distances when the solid curve (the energy in the central guide) is close to its maximum in Figure 9a and, at the same time, it approaches the minimum in Figure 9c. This optimal range of d values for NOT output is shown as shaded area in Figure 9. To achieve a NOR output, the solid curve in Figure 9b must be close to its minimum within the shaded area which is the case under the

chosen input conditions. The vertical dashed line in Figure 9 shows the optimal d value for implementation of NOR gate. The operation of NOT and NOR gate at this optimal d value is demonstrated in Figure 10. If both input packets are "000", the output is "111" (see Figure 10a); if both input packets are "111", the output of the gate is "000" (see Figure 10d). This corresponds to a NOT gate operation. In addition to this, if one of the input packets is "111" and another one is "000", the output is "000" (see Figures 10b and 10c). This corresponds to a NOR gate operation.

Operating characteristics of the resonant soliton logic gates

The main advantage of the resonant soliton switches and logic gates is their extremely high processing speed. They allow all-optical signal processing of ultra-high-bit-rate data streams in Tbit/s regime. To our knowledge, this is the only all-optical scheme proposed so far which permits execusion of AND, OR, XOR, NOT, NOR, and NAND logic functions with Tbit/s operating speed.

In the performed numerical simulations, the operating speed of all constructed logic gates is 2 Tbit/s. The operation is bit-rate flexible; this means that the logic gates will perform in the same way if the bit rates of the input data streams are increased or decreased. The maximum operating speed, however, is limited by two major factors. On the one hand, the time delay between the consecutive input pulses must be longer than 3τ where τ is the pulse duration, otherwise, the device performance degrades considerably. In the case $\tau = 100$ fs, which has been chosen in our numerical simulations, the maximum operating speed of the gates is ~ 3 Tbit/s. A higher operating speed can be achieved with a shorter input pulse duration; for example, if $\tau = 30$ fs, the operating speed can be as high as 10 Tbit/s. There is, on the other hand, also a limit on τ values which is implied by a choice of the particular semiconductor material used to fabricate the constituent waveguides of NLDC: the spectral width of the input pulses must be smaller than the binding energy of the excitonic transition of interest, otherwise, an excitation of the continuum states leads to rapidly increasing dephasing rates which significantly degrade the operating performance of switches and logic gates. In the case of II-VI CdZnTe/ZnTe MQWs, the exciton binding energy is ≈ 23 meV [2] which is large enough to allow the use of 100 fs pulses. In the case III–V GaAs/AlGaAs MQWs, the typical values of the exciton binding energy is smaller than 10 meV [2].

The signal-to-noise ratio (SNR) differs for different logic gates. Generally, it is in the range 4 – 10.

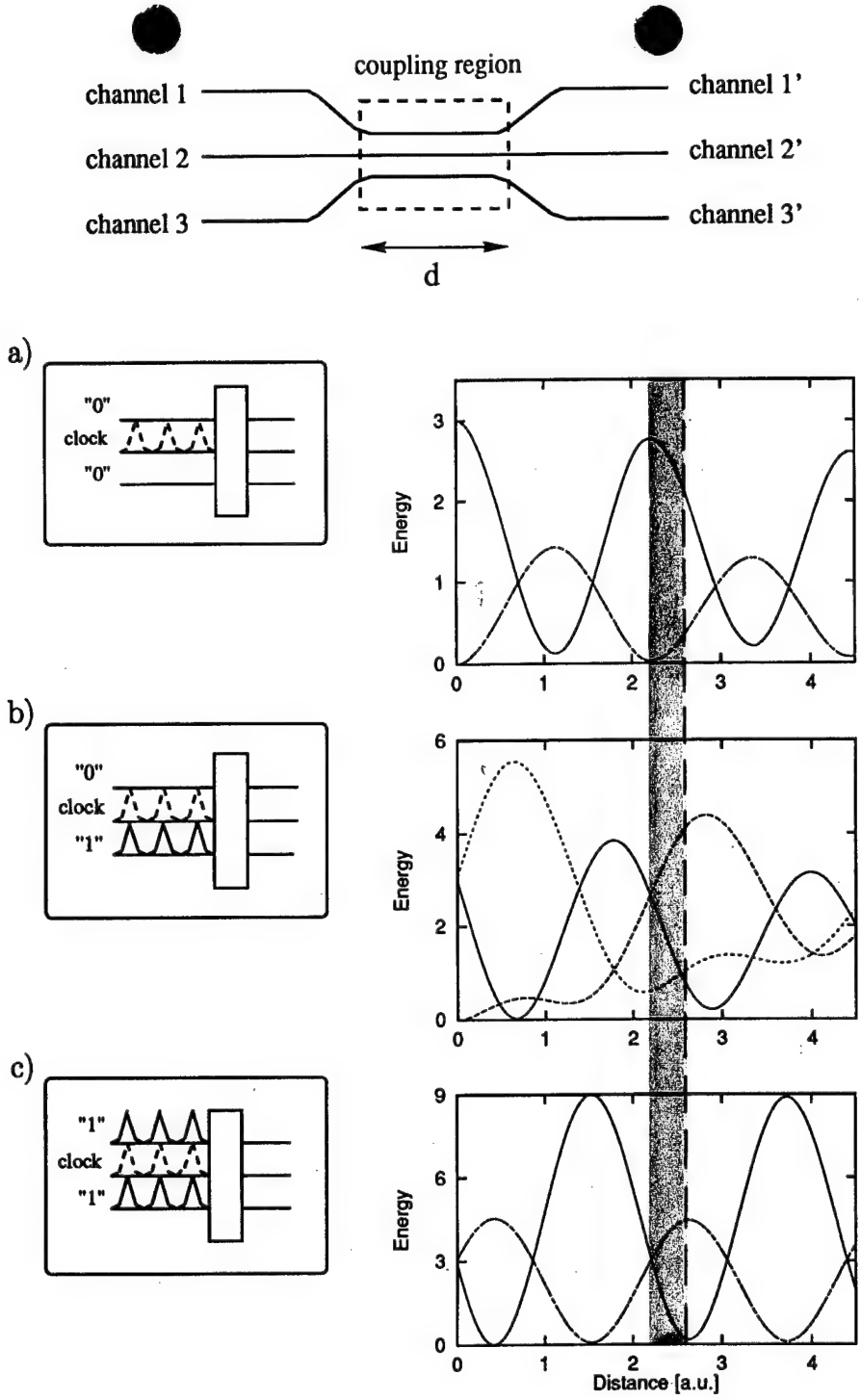


FIG. 9. Top: Schematic of 3 × 3 NLDC. Below: The energy exchange between the channels in 3 × 3 NLDC vs. propagation distance. Channels 1 and 3 are the input ports of NLDC, channel 2 supplies the clock stream. The inputs are given by three-bit packets. The input phase mismatch conditions are $\Delta\phi_{12} = \Delta\phi_{32} = -\pi/2$, $\Delta\phi_{13} = 0$. All energy values are normalized to the energy of a single pulse. The energy in channel 2′, 1′, and 3′ is shown by solid, dashed, and dotted lines, respectively. The input is: (a) "00"; (b) "01"; (c) "11". Note that the dashed and dotted lines overlap in the cases (a) and (c). The shaded region shows the range of d values suitable for realization of NOT gate; the vertical dashed line shows the optimal d value for realization of NOR gate.

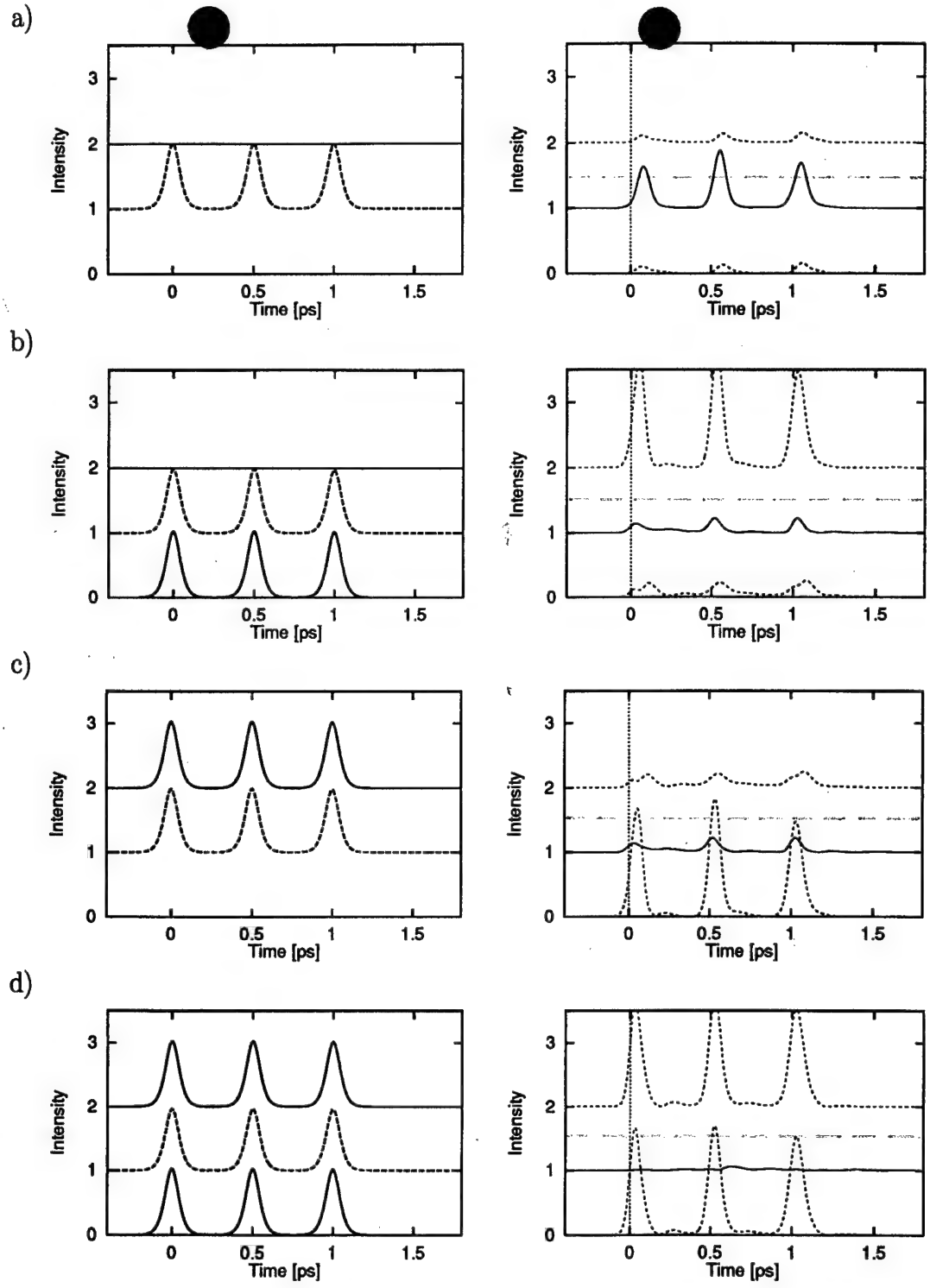


FIG. 10. NOT and NOR gate operation using a 3×3 NLDC. The input is shown on the left side: channels 1 and 3 are the input ports of the gate (solid line), channel 2 supplies the clock stream (dashed line). The input phase mismatch conditions are $\Delta\phi_{12} = \Delta\phi_{32} = -\pi/2$, $\Delta\phi_{13} = 0$. The output is shown on the right side: channel $2'$ is the output port of the gate (solid line), the signals in channels $1'$ and $3'$ are discarded (dotted line). The horizontal green line shows a threshold for amplitude detection. (a) The input is "00", the output is "11". (b) The input is "01", the output is "00". (c) The input is "10", the output is "00". (d) The input is "11", the output is "00". NOT gate operation is shown in (a) and (d). NOR gate operation is shown in (a)-(d).

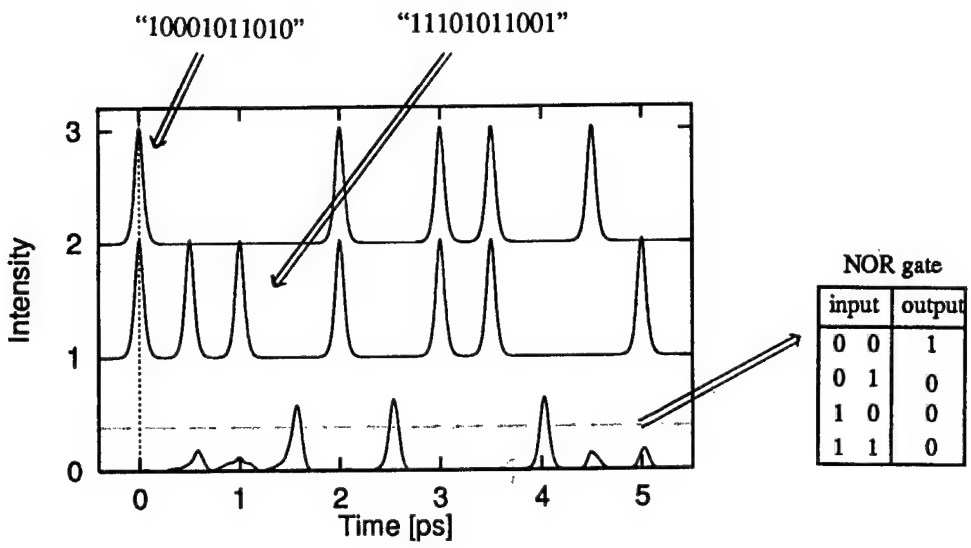


FIG. 11. NOR gate operation using a 3 × 3 NLDC and the corresponding truth table. The input logic stream 1 is given by an 11-bit packet "10001011010" (top); the input logic stream 2 is given by an 11-bit packet "11101011001" (middle); NOR output of the gate (bottom). The horizontal green line shows a threshold for amplitude detection.

The amplification procedure (logic level restoration) may lead to decrease in SNR value if the required gain factor exceeds two. This can be seen, for example, in Figure 6, NOT with gain, where SNR value decreases to 3 after the amplification while it was much higher before the amplification (NOT without gain). Note that SNR can be increased, if necessary, by optimizing the input pulse paramerters and structural device characteristics. For example, in the case of NOT and NOR gates using 3 × 3 NLDC, SNR value depends considerably on the length of the coupling region of the gate, d, which should be optimized (see Figure 9).

The pulse area of the standard "1" bits has been chosen to be 2π in our simulations. The corresponding pulse energy can be calculated if the value of the transition dipole moment is known. From relevant experimental results on soliton-like propagation of femtosecond optical pulses in the excitonic spectral region of bulk $CdSe$ [7], some numbers can be obtained. A set of measurements in Ref. [7] has been performed with 180 fs pulses, and the typical input pulse intensities have been 46 MW/cm^2 ($\sim 2\pi$ pulse area) and

26 MW/cm^2 ($\sim 1.5\pi$ pulse area). Note that these results have been obtained in 3D case and therefore cannot be quantitatively applied to 2D case which is of interest here. Other relevant experimental results have been reported in Ref. [6] where subpicosecond optical switching in GaAs/AlGaAs NLDCs with current injection has been studied. The results of a few measurements without injected current in the resonant excitation regime indicate that, in the case of GaAs/AlGaAs MQWs, the required pulse energy for the resonant switching should be below 20 pJ.

An important feature of the resonant soliton switches and logic gates is their compactness which results in low latency time. The typical device length for a semiconductor NLDC is about 1 mm (see, for example, Ref. [6]). The latency time of a resonant soliton logic gate depends not only on the device length, but also on the input pulse duration, τ. This is because the group velocity of the pulse under the resonant excitation conditions depends on τ: a shorter pulse propagates faster (see, for example, Ref. [8]). For 100 fs pulses, the latency time of a 1 mm coupler is about 40 ps. If a cascade of couplers is used to implement the gate (as in the case of NOT, NOR, and NAND gates using 2×2 device configuration), the latency time increases accordingly.

5. Comparison between performance of optical and electronic logic gates

First, we briefly review one of the most well-studied previous approaches to implement ultrafast all-optical logic gates. It is based on the effect of soliton dragging in optical fibers [9]. In the temporal soliton dragging, two solitons propagate in a birefringent optical fiber and interact through cross-phase modulation. This causes a chirp in the carrier frequency and a time shift pulling the signal out of the clock time window. The operation of all-optical AND, OR, and NOR gates based on soliton-dragging in fibers have been demonstrated experimentally [9,10]. These gates can operate at bit rates up to 0.2 THz, are phase-insensitive, cascadable, and can be implemented with gain. However, there are several physical factors which severely limit their performance: timing jitter, very long latencies (hundreds of nanoseconds), technical complexity of the time window detection (ultrafast temporal coincidence [9]), high switching energy, strong output signal distortion, high losses, etc. The switching energy can be decreased by using low-birefringent (low-bi) optical fibers which allow to achieve a longer interaction length between two orthogonally polarized pulses in the nonlinear optical loop mirrow configuration (NOLM) [11]. The AND, XOR, and NOT gates have

been constructed using the low-bi NOLM scheme, but they show a very different performance. For example, the switching contrast ratio of NOT and XOR gates degrades 8 times in comparison with AND gate [11]. Overall, the further significant efforts are required to improve performance of the NOLM scheme and to make it viable for applications in serial data processing.

The resonant soliton scheme which we exploit is based on a fundamentally different physical approach. Instead of time shifts from the soliton dragging, we use a change in the pulse amplitude due to interaction of two phase-mismatched solitons. The required phase mismatch of $\pi/2$ is easy to implement experimentally. The major advantages of the resonant soliton scheme in comparison with the non-resonant schemes such as NOLM have been discussed in our previous work in the contest of switching [1], and they hold true in the case of optical logic. The most important advantage is the speed of signal processing. We have demonstrated numerically that the resonant soliton logic gates operate at bit rates as high as 2 THz exceeding the maximum speed of data processing with the soliton dragging gates by an order of magnitude. At the same time, the semiconductor logic gates are very compact; typically, the length of the coupler does not exceed 1 mm resulting in low latency time (tens of picoseconds) which is at least four orders of magnitude better than the typical latencies of NOLM setups. Our approach also eliminates the necessity for complex time window detection technique replacing it by a simple amplitude threshold detection. Overall, on the basis of our numerical results, we conclude that the resonant soliton logic gates outperform the soliton-dragging gates, however, an experimental investigation of the resonant soliton scheme should follow to support this conclusion.

To compete successfully with the electronics, optical logic gates must be able to perform the same functions as the electronic gates with comparable or better operating characteristics. In our numerical work, it has been demonstrated that the resonant soliton logic gates satisfy the fundamental requirements for digital optical logic devices (logical completeness, cascadability, and logic level restoration). An operation of all-optical AND, OR, XOR, NOT, NOR, and NAND gates has been modelled. This proves that the resonant soliton logic gates have the same functionality as the electronic gates.

Although it is difficult to provide precise limits on the minimum achievable switching time, switching energy, and other operating characteristics for semiconductor electronics technology, which continues to advance rapidly, the following bounds are representative of the order of magnitude:

Minimum switching time = 10 – 20 ps

Minimum energy per operation = 10 – 20 fJ

Minimum switching power = 1 μW.

We have demonstrated numerically that the minimum switching time with the resonant soliton scheme is on femtosecond timescale. This means that the resonant soliton switches and logic gates are capable to operate at least 100 times faster than the most advanced electronic switches. The switching speed of 2 Tbit/s, demonstrated in our numerical simulations, cannot be attained by semiconductor electronic switches. Such a speed is also beyond the present capabilities of Josephson devices.

The energy consumption of the optical switches can be, in principle, smaller than in semiconductor electronics. Due to the lack of direct experimental results on a switching power in the resonant soliton NLDC, quantitative comparison cannot be presently made. In our numerical simulations with 2π pulses, the estimated energy per operation exceeds the minimum energy consumption of electronic switches. Any attempts to optimize the energy consumption of the resonant soliton gates are beyond the scope of the present work.

An important feature of the resonant soliton logic gates is their compactness. A width of the constituent waveguides in a typical semiconductor NLDC is about 3 μm, the spacing between them is 2 μm, and a length of the NLDC can be as small as 1 mm (see, for example, Ref. [6]). This leads to a low latency time of about tens of picoseconds whereas the typical latencies of the electronic gates are on nanosecond timescale.

The numerical results which have been obtained during the course of this work allow us to conclude that the resonant soliton logic gates represent a novel and unique class of all-optical devices which are capable to compete successfully with the electronic logic gates. A range of potential applications of these novel devices is vast and covers areas such as ultrafast optical processing in time-division-multiplexed (TDM) networks, high-speed optical logic, optical packet routing, optical data stream encryption, optical computing, ultrafast data processing in satellite communications, etc. At the present stage, it is highly desirable to initiate an experimental investigation of the resonant soliton switching scheme to be carried out in parallel with theoretical research.

6. Summary

- The issues of logic level restoration, cascadability, and logical completeness with the resonant soliton scheme have been addressed. It has been proved that the resonant soliton switches meet all three above requirements for digital optical logic devices.

- The operation of AND, OR, XOR, NOT, NOR, and NAND logic gates have been demonstrated in numerical simulations using 2×2 device configuration for a directional coupler.

- 3×3 NLDC design has been suggested to implement logically complete gates without necessity to cascade two or more couplers. An extended numerical code describing the operation of 3×3 NLDC has been developed and tested. Using 3×3 device configuration, the operation of an inverter (NOT gate) and a NOR gate have been demonstrated.

- The operating characteristics of the resonant soliton logic gates have been investigated numerically using 100 fs input pulses with 2π pulse area. It has been shown that the operating speed of all constructed gates is 2 Tbit/s, the operation is bit-rate flexible, the signal-to-noise ratio is generally higher than 4, and the latency is on picosecond timescale.

- Quantitative comparison between the operating characteristics of the resonant soliton logic gates and the corresponding parameters of NOLM gates (fiber optics) and also semiconductor electronic logic gates has been made. A conclusion has been drawn that the resonant soliton logic gates represent a novel and unique class of all-optical devices which are capable to operate at least 100 times faster than the most advanced electronic switches and logic gates.

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